

IEC 61131-3 Compliant Programmable Logic Controller

# EHV+ Series

Powered by CoDeSys

**HITACHI**  
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## *Powerful general purpose PLC*



# Powerful and flexible

## Hitachi EHV+ Series

Core of the new powerful general purpose EHV+ CPU series is the CoDeSys V3 runtime system. The result is an open and flexible system which is completed through utilising existing EH-150 modules.



EH-150 system incl. EHV+ CPU and various I/O modules



### Memory capacity

- User program (RAM) up to 1024 kByte
- Boot project (FLASH) up to 1024 kByte
- Source file (FLASH) up to 6 MByte
- Data memory 256 kByte

### Communication interfaces

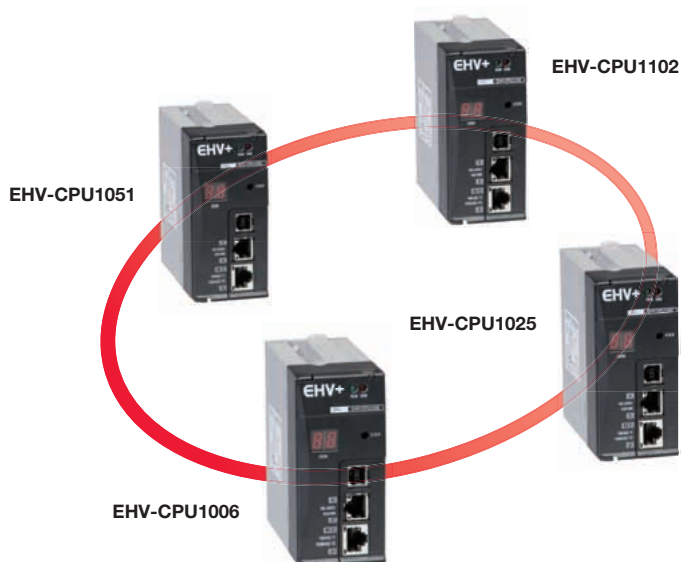
- Ethernet (10BASE-T/100BASE-TX)
- USB interface (Ver. 2.0 Full speed 12 Mbps)
- Serial interface (RS-232C/RS-422/RS-485)

### Programming

- Communication protocol CoDeSys V3
- Programming languages according to IEC 61131-3: LD, IL, FBD, ST, SFC, CFC

### Communication protocols

- Modbus TCP Client
- Modbus RTU Master



### EHV+ CPU module

The new EHV+ series consists of 4 powerful CPUs. The models differ through memory capacities (64, 256, 512, 1024 kByte) whilst maintaining a consistently high performance. The EHV+ CPU is compatible with a variety of open networks through use of the onboard Ethernet interface.

### Programming software EHV-CoDeSys

Thanks to full compliance to the IEC 61131-3 standard, the user can select among 6 programming languages (LD, IL, FBD, ST, SFC, CFC) in EHV-CoDeSys. In addition to the PLC programming functionality, EHV-CoDeSys offers powerful visualisation functions such as an integrated graphical editor, which is useful for testing, commissioning or diagnostic purposes.

# Easy and efficient

## Flexible choice

Flexible choice of editors and usage of library functions considerably decreases programming time

The screenshot displays the CoDeSys IDE interface for a project named 'SCF\_sample\_R01.project'. It features a multi-view editor with four main panes:

- Top-left:** Ladder logic diagram showing an AND block with inputs 'switch1' and 'switch2', followed by an OR block with input 'sta\_l4\_covyr', leading to a TON (Timer On Delay) block. Below it, another TON block is shown with inputs 'BI\_sta\_flag' and 'NOT switch2'.
- Top-right:** STL (Staircase Ladder) code snippet:

```
CALL TON_T1(  
  IN:= ton_input,  
  ET:= T#30000,  
  ET:= ton_etp)  
LD ton_output  
LD Lift_A  
OR sta_l4_covyr  
ST IL_sample_out
```
- Bottom-left:** Text editor showing a complex STL program with conditional logic and timer management:

```
1 L2_wait_timer (I1:= 1, ET:= T#1000);  
2 // L2_wait_timer();  
3 elp_wait:= L2_wait_timer.ET;  
4  
5 IF elp_wait > T#30 THRESH  
6   test_out5:=1;  
7   IF elp_wait > T#100 THRESH  
8     test_out5:=1;  
9   IF elp_wait > T#150 THRESH  
10    test_out5:=1;  
11   IF elp_wait > T#200 THRESH  
12     L2_wait_timer (I1:=0);  
13     test_out5:=0;  
14     test_out10:=0;  
15     test_out15:=0;  
16   END_IF  
17 END_IF  
18 END_IF  
19  
20 L2_wait_timer (in:=1);
```
- Bottom-right:** Ladder logic diagram showing a RTON (Timer Reset On Delay) block with inputs 'STA\_S1\_pump' and 'NOT R3\_sta\_flag', leading to 'stp\_I'. A timer 'T#0.5s' is also shown.

## Fast and convenient

Fast and convenient debugging/testing during commissioning

The screenshot shows the CoDeSys IDE in a debugging or monitoring mode. The top-left pane displays the ladder logic diagram with real-time values overlaid on the logic elements:

- Inputs 'switch1' and 'switch2' are shown as 'TRUE'.
- The output of the AND block is 'TRUE'.
- The output of the OR block is 'FALSE'.
- The output of the TON1 block is 'TRUE'.
- The output of the NOT block is 'TRUE'.
- The output of the TON2 block is '#10.00ms'.

The bottom-left pane shows the STL code with corresponding values overlaid on the expressions:

- 'elp\_wait' is '#10.00ms'.
- 'test\_out5' is 'FALSE'.
- 'test\_out10' is 'FALSE'.
- 'test\_out15' is 'FALSE'.

The Messages window at the bottom indicates a successful build: 'Build complete -- 0 errors, 0 warnings: ready for download!'.

## Specifications

Type		EHV-CPU1006	EHV-CPU1025	EHV-CPU1051	EHV-CPU1102
Processing speed		145 ns/instruction	145 ns/instruction	145 ns/instruction	145 ns/instruction
Memory	User program (RAM)	64 kByte	256 kByte	512 kByte	1024 kByte
	Boot project (FLASH)	64 kByte	256 kByte	512 kByte	1024 kByte
	Source file (FLASH)	2 MByte	6 MByte	6 MByte	6 MByte
	Data memory	256 kByte	256 kByte	256 kByte	256 kByte
	Retain data memory	16 kByte	16 kByte	16 kByte	16 kByte
Supported expansion bases		0	5	5	5
Fieldbus memory		16 kByte (2 kByte × 8 units)			
Processing method		Refresh			
Programming software		EHV-CoDeSys (Version 3.4)			
Programming languages		LD, IL, FBD, ST, SFC, CFC (Continous Function Chart)			
Communication port		CoDeSys V3 protocol			
USB	2.0, Full speed	Programming			
Ethernet	UDP/IP, TCP/IP	Programming / General purpose / Modbus TCP Client / Ethernet IP (under development)			
Serial	RS232C/422/485	Programming / General purpose / Modbus RTU Master			
User Interface	Display	RUN LED, ERR LED, 7-segment LED			
	Run switch	Remote RUN/STOP (RUN position)			
	E.CLR switch	Clear error indication in 7-segment LED			
RTC		Supported (access by RTC FB)			
Battery		Built-in (LIBAT-H)			
Approval		CE, UL, cUL, C-Tick			

## EHV-CoDeSys

Item		Descriptions
System requirements	RAM	1 GB
	Operating System	Windows 2000 or higher (not yet released for the 64-bit platforms of Windows Vista and Windows 7)
	CPU	1 GHz Pentium
	Hard disk	1 GB
	Screen resolution	1024 × 768
Communication cables	USB	Standard USB cable (Type B connector)
	Ethernet	UTP or STP cable (cat5E)
	Serial	EH-PROG40

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